AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

11. (Currently Amended) A high swing cascode biasing circuit, comprising:

a current biasing circuit that generates a cascode bias and a main bias;

a frequency boosting circuit that receives said cascode bias and said main bias; and

a current mirror circuit that receives said main bias, wherein said frequency boosting circuit biases said current mirror and receives feedback from said current mirror.

12. (Original) The high swing cascode biasing circuit of Claim 11 wherein said current mirror circuit includes a first transistor, a second transistor and a first capacitance having one end connected between said first and second transistors and wherein said frequency boosting circuit biases a control terminal of said first transistor and receives feedback from said one end of said first capacitance.

13. (Original) The high swing cascode biasing circuit of Claim 12 wherein said frequency boosting circuit comprises:

a third transistor that has a control terminal that receives said cascode bias, a first terminal and a second terminal; and

a fourth transistor that has a control terminal that receives said main bias, a first terminal that communicates with said second terminal of said third transistor and a second terminal.

14. (Original) The high swing cascode biasing circuit of Claim 13 wherein said frequency boosting circuit comprises a second capacitance having one end that communicates with said first terminal of said third transistor and an opposite end that communicates with said second terminal of said third transistor and with said one end of said first capacitance.

15. (Original) The high swing cascode biasing circuit of Claim 14 wherein said frequency boosting circuit comprises an inverter that has an input that communicates with said first terminal of said third transistor and an output that communicates with said control terminal of said first transistor.

16. (Original) The high swing cascode biasing circuit of Claim 15 wherein said frequency boosting circuit comprises a first resistance having one end that communicates with said input of said inverter and an opposite end that communicates with said output of said inverter.

17. (Original) The high swing cascode biasing circuit of Claim 12 wherein said first and second transistors are metal-oxide semiconductor field-effect transistors (MOSFETs).

18. (Original) The high swing cascode biasing circuit of Claim 12 wherein said feedback increases a transconductance of said first transistor.

19. (Original) The high swing cascode biasing circuit of Claim 11 wherein said frequency boosting circuit increases a bandwidth of said high swing cascode biasing circuit.

20. (Original) An Ahuja compensation circuit comprising the high swing cascode biasing circuit of Claim 11.

21. (Currently Amended) A high swing cascode biasing circuit, comprising:

current biasing means for generating a cascade bias and a main bias;

frequency boosting means for receiving said cascode bias and said main bias and for boosting a frequency response of said high swing cascode biasing circuit; and

current mirror means for receiving said main bias, wherein said frequency boosting means biases said current mirror means and receives feedback from said current mirror means.

22. (Original) The high swing cascode biasing circuit of Claim 21 wherein said current mirror means includes a first transistor, a second transistor and first capacitance means for providing a first capacitance and having one end connected between said

first and second transistors and wherein said frequency boosting means biases a control terminal of said first transistor and receives feedback from said one end of said first capacitance means.

23. (Original) The high swing cascode biasing circuit of Claim 22 wherein said frequency boosting means comprises:

a third transistor that has a control terminal that receives said cascode bias, a first terminal and a second terminal; and

a fourth transistor that has a control terminal that receives said main bias, a first terminal that communicates with said second terminal of said third transistor and a second terminal.

24. (Original) The high swing cascode biasing circuit of Claim 23 wherein said frequency boosting means comprises second capacitance means for providing a second capacitance and having one end that communicates with said first terminal of said third transistor and an opposite end that communicates with said second terminal of said third transistor and with said one end of said first capacitance means.

25. (Original) The high swing cascode biasing circuit of Claim 24 wherein said frequency boosting means comprises inverting means for inverting that has an input that communicates with said first terminal of said third transistor and an output that communicates with said control terminal of said first transistor.

26. (Original) The high swing cascode biasing circuit of Claim 25 wherein said frequency boosting means comprises first resistance means for providing a first resistance and having one end that communicates with said input of said inverter and an opposite end that communicates with said output of said inverter.

27. (Original) The high swing cascode biasing circuit of Claim 22 wherein said first and second transistors are metal-oxide semiconductor field-effect transistors (MOSFETs).

28. (Original) The high swing cascode biasing circuit of Claim 22 wherein said feedback increases a transconductance of said first transistor.

29. (Original) An Ahuja compensation circuit comprising the high swing cascode biasing circuit of Claim 21.